CS 631-02 Digital Design
Sequential Logic

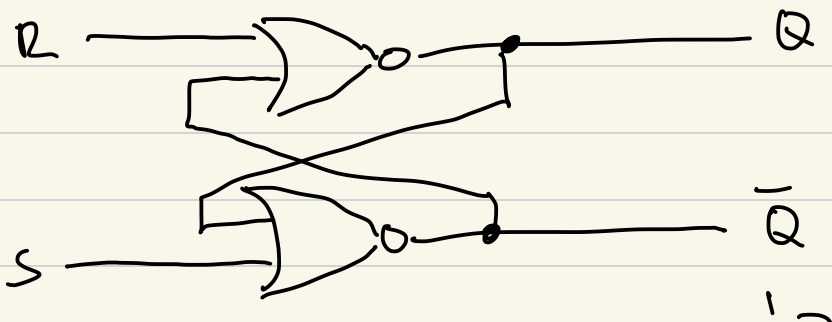
Lab06 Testing

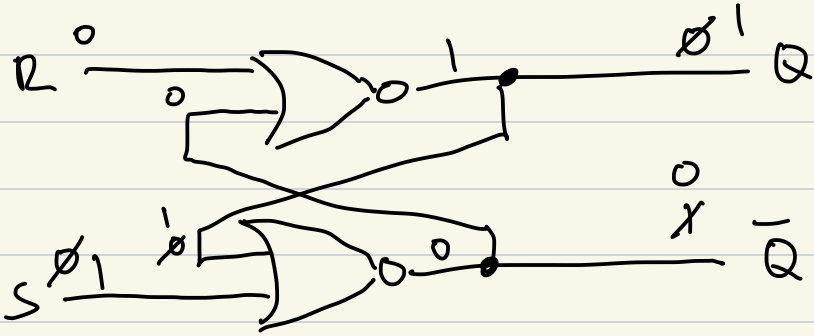
Goal: Build an N-bit Register

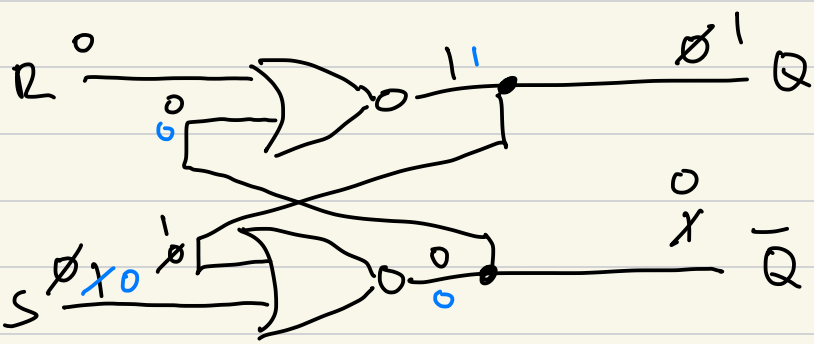
SR Latch
↓
Clock
↓
D Latch
↓
D Latch with CLR
↓
Multiplexors
↓
D flip-flop
↓
D flip-flop with CLR and EN → 1 bit register

SR latch Set Reset

Static RAM

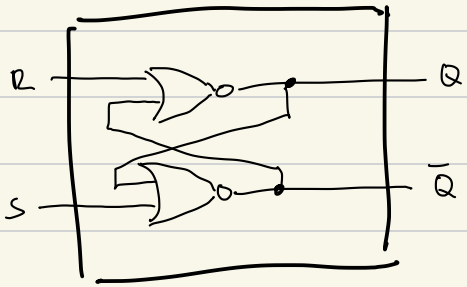




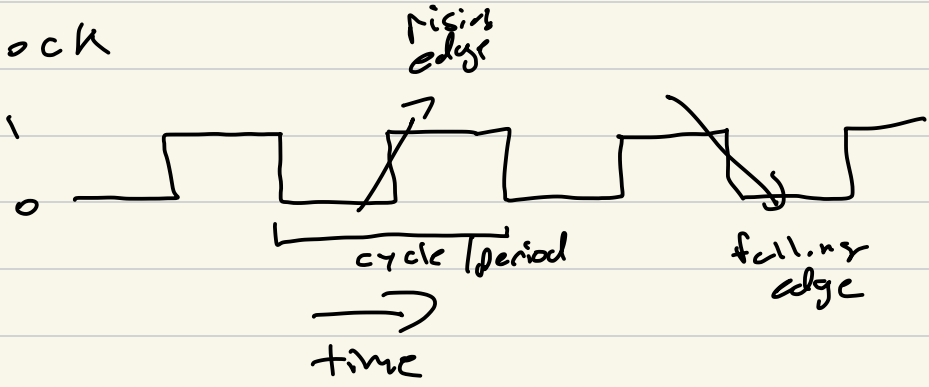


R S	Q $\bar{Q}$
0 0	0 1
0 1	1 0
0 0	1 0
1 0	0 1
0 0	0 1
1 1	X X

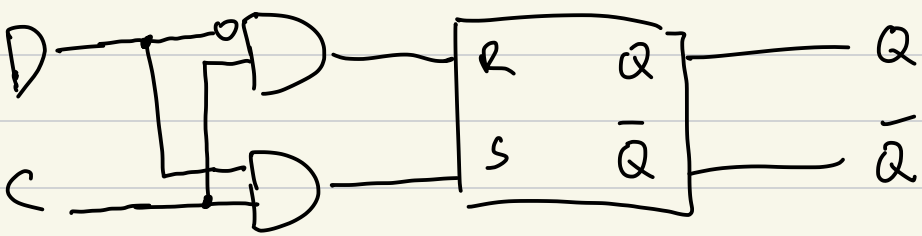
SR Latch



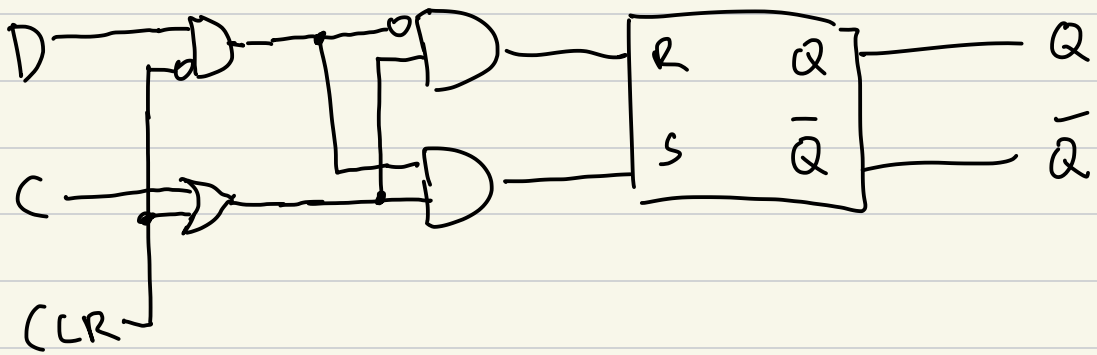
Clock



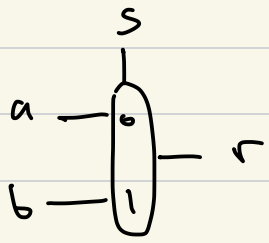
D Latch

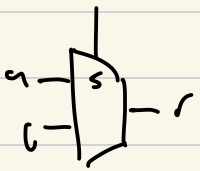


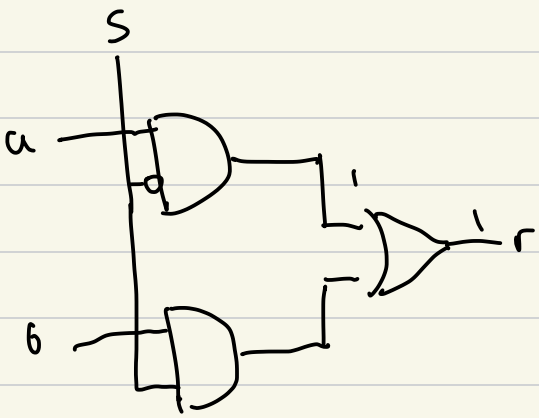
D Latch with CLR



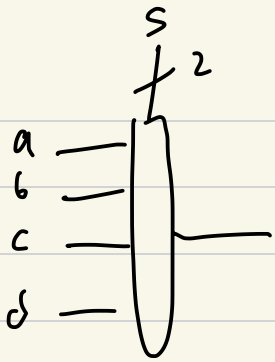
Multiplexors

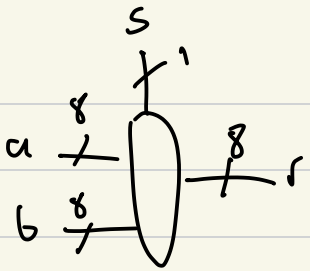


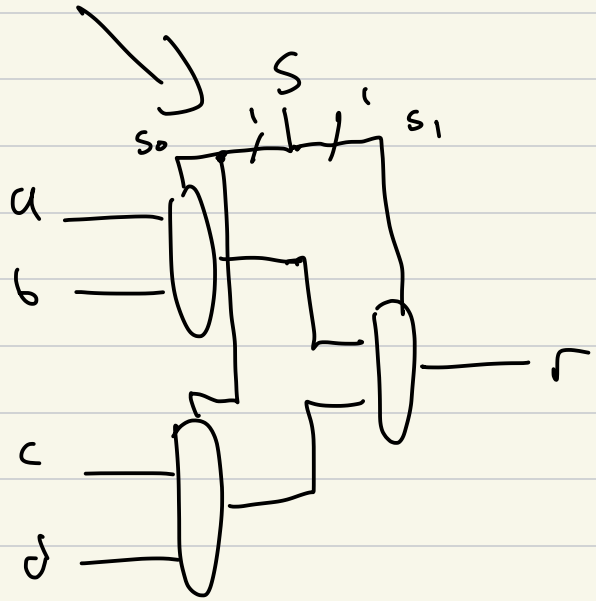




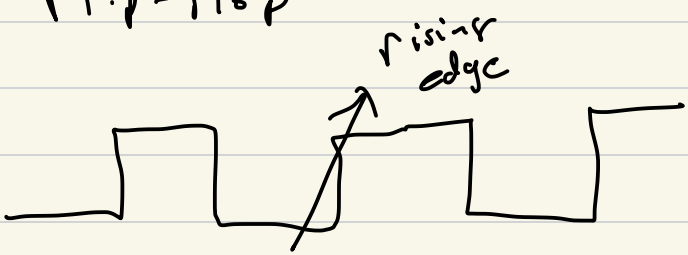
a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

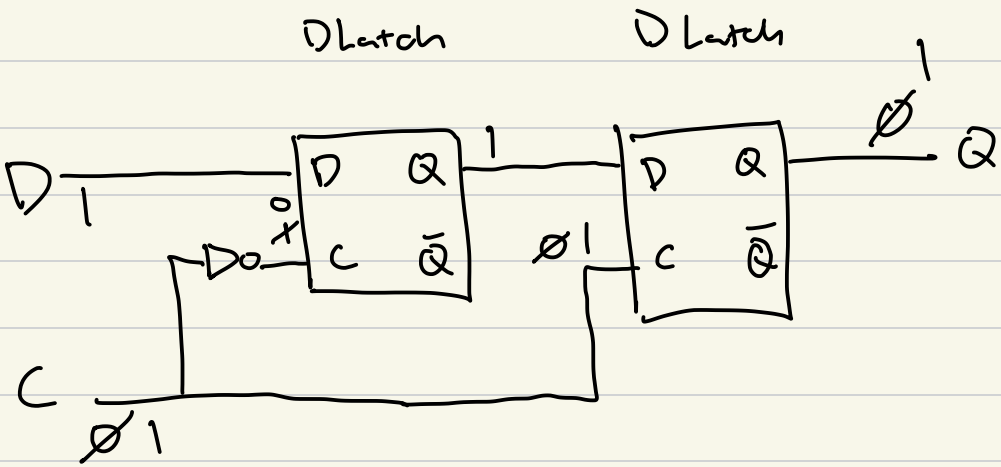

S
2
a
b
c
d


S
1
a
8
b
8
8
r


S
S0
S1
a
b
c
d
r

D flip-flop


rising edge


D Latch
D Latch
D
1
0
D
Q
C
$\bar{Q}$
1
ϕ 1
ϕ 1
C
ϕ 1
ϕ 1
Q

D flip-flop with CLR and EN